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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
TON, DAVID	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 09/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/626,728	LOUGHMILLER, DANIEL R.	
	Examiner	Art Unit	
	David Ton	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment filed on 06/22/2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13 and 15-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 15-66* is/are rejected.

7)☒ Claim(s) *15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

1. Applicants Amendment filed on 06/22/2006 has been reviewed.

2. Applicant's arguments with respect to claims 1-13 and 15-66 have been considered but are moot in view of view of the new ground(s) of rejection.

3. Claims 1-13 and 15-66 are presented for examination.

Claim Objections

4. Claims 15 and 16 are objected to because they are dependent from a canceled claim (claim 14).

Claim Rejections - 35 USC ' 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

6. Claims 1-5, 7-13, 17-18, 22-25, 27-29, 42, and 46-48 are rejected under 35 U.S.C. § 102(e) as being anticipated by Towler et al. (Towler) patent no. 6,618,279 (art provided in previous Office Action in PTO 892).

7. As to claim 1, Towler teaches the invention as claimed, including a test circuit [see Fig. 5 and col. 5 lines 25-36] for testing a match detection circuit, comprising:

A test line [TO of Fig. 5] for providing a load [transistors 31 of Fig. 5] to the match detection circuit [Fig. 5], said test line being switchably [see claim 3 coupled to a first line of the match detection circuit to provide the load [see claim 1] on the first line to test a feature ["evaluation", see col. 6 lines 15-68] of the match detection circuit.

8. As to claims 2-3, Towler teaches the first line of match detection circuit comprises a match line [[line ML of Fig. 2] and a discharge line [line connecting T6 to ground of Fig. 2].

9. As to claim 4, Towler teaches the test line comprises a test line switch [transistor TO of Fig. 5] couple between said load and said match detection circuit.

10. As to claim 5, Towler teaches a test circuit controller [see Fig. 4] for controlling said switch.

11. As to claims 7-8, Towler teaches a second test line [transistor T32 of Fig. 5] for providing second load to the match detection circuit and the second load is different from said first load [transistor T31 of Fig. 5].

12. As to claims 9-11, Towler teaches a third test line [transistor T33 of Fig. 5] for providing third load to the match detection circuit and the third load is different from said first load [transistor T31 of Fig. 5] and said second load [transistor T32 of Fig. 5].

13. As to claim 12, Towler teaches a test circuit for a detection match circuit comprising a test line being switchably coupled to a first line of a match detection circuit for providing a load to said match detection circuit [se claim 3].

14. As to claim 13, Towler teaches said test line comprises a load [transistor T31 of Fig. 5] and a test line transistor [transistor TO of Fig. 5].

15. As to claims 17-18, Towler teaches the first line of match detection circuit comprises a match line [[line MATCH of Fig. 5] and a discharge line [line connecting C0 to ground of Fig. 5].

16. As to claim 22, Towler teaches a test circuit for a match detection circuit comprising a test circuit for providing a first load to said match detection circuit to test a margin of said match detection circuit [col. 8 lines 10-22].

17. As to claims 23-25, Towler teaches a first test line [transistor T31 of Fig. 5], a second test line [transistor T32 of Fig. 5] for providing first load and a second load to the match detection circuit and the second load is different from said first load [transistor T31 of Fig. 5].

18. As to claim 27, Towler teaches a test circuit controller [see Fig. 6] for controlling said first load provided to said match detection circuit, said test circuit controller coupled to said gate of said test line transistor [lines P1-P4 of Fig. 5].

19. As to claims 28-29, Towler teaches a test circuit is switchably coupled to a matchline and discharge line [see claim 3].

20. As to claim 42, Towler teaches a method of testing a match detection circuit comprising steps of: switchably coupling a load to said match detection circuit; and applying said load to said match detection circuit to test a feature of the match detection circuit [see claim 1 and Fig. 5].

21. As to claims 46-48, Towler teaches the first line of match detection circuit comprises a match line [[line MATCH of Fig. 5] and a discharge line [line connecting C0 to ground of Fig. 5].

Claim Rejections - 35 USC ' 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 6, 15, 16, 19, 20, 21, 26, 30-41, 43-45, and 49-66 are rejected under 35 U.S.C. § 103 (a) as being unpatentable over Towler et al. (Towler) patent no. 6,618,279.

24. As to claim 6, Towler does not teaches using resistor for pull-up impedance. Instead, Towler teaches using transistors to provide the pull-up impedance.

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to enhance the teachings of Towler by using the pull up resistor for pull-up impedance because a resistor is a well known impedance. This modification would have been obvious and a person having ordinary skill in the art

would have been motivated to do so as a matter of design choice because it would provide the same impedance value for Towler circuit evaluation.

25. As to claims 15-16, Towler teaches said load comprises a voltage [VDD of Fig. 5] and a ground [ground of Fig. 5].

26. As to claim 19, Towler teaches test control line [lines P1-P4 of Fig. 5] for activating the transistor.

27. As to claim 20, Towler teaches a decision circuit [L1 of Fig. 5, see col. 6 lines 38-50].

28. As to claim 21, it is a matter of design choice to use a NOR circuit to implement the Towler decision circuit.

29. As to claim 26, Towler teaches a test line transistor for switchably coupling said test line to said match detection circuit [claim 3].

30. As to claims 30-31, Towler teaches a test circuit [Fig. 5] for testing a match detection circuit, said test circuit comprising:

A test circuit controller [Fig. 6];

A plurality of test lines switchably [claim 3] coupled to a matchline detection circuit to test a feature of said match detection circuit, wherein each of said plurality of test lines comprises:

A load [T31 of Fig. 5];

And a test line transistor [T0 of Fig. 5] coupled between said load and said matchline, a gate of said test line transistor coupled to said test circuit controller.

Towler does not teaches using resistor/voltage for pull-up impedance. Instead, Towler teaches using transistors to provide the pull-up impedance.

It would have been obvious to one of ordinary skill in the Data Processing art at the time of the invention was made to enhance the teachings of Towler by using the pull up resistor for pull-up impedance because a resistor is a well known impedance. This modification would have been obvious and a person having ordinary skill in the art would have been motivated to do so as a matter of design choice because it would provide the same impedance value for Towler circuit evaluation.

31. As to claims 32-41, they are similar to claims 30-31 above; therefore, it is rejected under the same rationale. Furthermore, Towler also teaches a decision circuit [L1 of Fig. 5], for CAM system [see abstract],

32. As to claim 43, Towler teaches comparing a store data bit in said match detection circuit with a comparand data bit [claim 1].

33. As to claims 44-45, Towler teaches applying a resistance/voltage to a first line of said match detection circuit [claim 1].

34. As to claims 49-66, Towler inherently teaches a method of testing a match detection circuit comprising steps of precharging, applying, comparing and determining [see claim 6-7] as set forth in the claims.

Conclusion

35. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ton whose telephone number is (571) 272-3828. The examiner can normally be reached on M-Th from 5:30 - 4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert DeCady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Ton
Primary Examiner
Art Unit 2138